Remarks/Arguments

This Amendment is in response to the Office Action mailed 9 June 2004 (09.06.2004).

In this Office Action, the Examiner rejected claims 1-20 under 35 USC 103(a). Specifically, the Examiner rejected claims 1, 2, 5-7, 10-12, 15-17, and 20 as being unpatentable over Hoffman et al. (US Pat. No. 6,513,089) and Akrout et al. (US Patent Application Publication No. 2003/0115500). The Examiner rejected claims 3, 8, 13, and 18 as being unpatentable over Hoffman and Akrout, in view of Sheafor et al. (US Patent No. 6,493,407), Quereshi et al. (US Patent No. 6,173,349), and Pawlowski et al. (US Patent No. 5,469,547). Finally, the Examiner rejected claims 4, 9, 14, and 19 as being unpatentable over Hoffman and Akrout, in view of Freidin et al. (US Patent No. 5,410,194.

1. Summary of Current Claims

Claims 21-40 remain in this application. Claims 1-20 have been canceled. Claims 21-25 are drawn to a method to manufacture a System-on-Chip (SOC) apparatus having a latency-tolerant architecture, and are somewhat commensurate in scope to original claims 11-15. Claims 26-30 are drawn to a method to use a System-on-Chip (SOC) apparatus having a latency-tolerant architecture, and are somewhat commensurate in scope to original claims 16-20. Claims 31-35 are drawn to a System-on-Chip (SOC) apparatus, and are somewhat commensurate in scope to original claims 1-5, and claims 36-40 are drawn to a system that includes a System-on-Chip apparatus, and are somewhat commensurate in scope to original claims 6-10.

2. Claim Rejections under 35 USC 103(a)

The Examiner rejected claims 1, 2, 5-7, 10-12, 15-17, and 20 as being unpatentable over Hoffman et al. (US Pat. No. 6,513,089) and Akrout et al. (US Patent Application Publication No. 2003/0115500). In response to the Office Action, Applicant is amending and reordering the claims to further clarify the claimed invention. Applicant believes that a new search is unnecessary as these amendments narrow the scope of the claimed invention. Further, Applicant believes that these amendments place the pending claims in immediate condition for allowance or appeal.

The Examiner asserts that Hoffman teaches an SOC apparatus that includes a processor core, one or more peripherals, and a first internal bus that couples the processor core and peripherals and carries signals from signal initiators to signal targets. The Examiner concedes that Hoffman does not teach the use of a latency tolerant signal protocol that allows an arbitrary number of pipeline stages between any signal initiator and any signal target, but states that Akrout does, citing Fig. 4 and Page 3, paragraph 27. The Examiner asserts that combining Hoffman's SOC architecture with Akrout's pipelined bus would be obvious to one of ordinary skill in the art, because "a pipelined bus beneficially improves the speed (frequency) at which the bus may be operated", citing Akrout page 3, paragraph 27. The Examiner applies the same logic to find that the combination of Hoffman and Akrout teach the system (original claim 6), the method of making the apparatus (original claim 11), and the method of using the apparatus (original claim 16).

Applicant agrees that as a general matter, there are speed benefits to using a pipelined bus, and that adding pipeline stages to achieve speed benefits are well known to those of ordinary skill in the art of processor design. Indeed, the instant application provides a much more thorough description of the use of pipelined buses and the benefits that can be achieved by such use than the description provided by Akrout. See Application, page 4, line 15 through page 7, line 9. As these paragraphs describe, pipelining a bus to enable higher-speed operation has a number of drawbacks, including introducing stalling opportunities (p. 5 l. 6), creating logic and timing synchronization problems (id. at l. 11-13), and necessitating multiple iterations of design and floorplanning (id. at l. 13-15). The instant application describes approaches that processor designers who employ pipelined buses have typically taken to minimize these drawbacks, noting that workarounds commonly used for processor designs in the past are not useful in an SOC environment because SOC size, transistor locations, and operating frequencies are not fixed and known until after the SOC is floorplanned. See Application p. 6, line 8 –p. 7, line 9. As this discussion demonstrates, pipelining a bus in an SOC environment such as that taught by Hoffman is not an obvious modification, because of the significant drawbacks—most notably, necessitating iterative design and floorplanning—that pipelining introduces.

Akrout's disclosure, which is a processor design that includes a pipelined bus embodiment, does not teach, suggest, or imply the use of any special technique or design workaround to use in conjunction with the pipelined bus to minimize drawbacks. Moreover, Akrout is describing a processor system having a certain number of

functionally equivalent redundant processors connected via a pipelined bus. Processor designers practicing Akrout's invention have necessarily pre-selected the number of redundant processors they intend to include in their design, and therefore, have pre-selected the number of pipeline stages that will be included on the bus. Consequently, Akrout is simply describing the use of a fixed pipeline depth, which is well known in the art of processor design and described in the instant application at p. 5, l. 18-p. 6, l. 2. Akrout does not teach the use of an arbitrary number of pipeline stages, within the meaning and intent of Applicant's use of the phrase "arbitrary number of pipeline stages."

MPEP 2143 requires that to establish a prima facie case of obviousness, an Examiner must met three basic criteria:

> First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

Moreover, MPEP 2141 states that references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination, References must be viewed without the benefit of impermissible hindsight, and MPEP 2141 reiterates that there must be a reasonable expectation of success.

Most of these criteria are not met by the combination of Hoffman and Akrout. As described above, Akrout describes the use of a fixed-depth pipeline in a processor design. There is nothing in Akrout's disclosure that teaches the use of a non-fixed-depth pipeline having an arbitrary number of stages in a non-processor application.

Likewise, there is nothing in Akrout's disclosure that teaches practitioners how to overcome the many drawbacks of using a pipelined bus of indeterminate depth in their designs. Consequently, those skilled in the art would not be motivated to combine the reference teachings and use a pipelined bus having an arbitrary number of pipeline stages in a non-processor application, because there would not be a reasonable expectation of achieving success.

Notwithstanding the above, Applicant has canceled the original claims and added new claims that more clearly point out and claim the novel features of the present invention, most notably, the capability of the present invention to enable the addition of an arbitrary number of pipeline stages at floorplanning without requiring further design iterations. Neither Hoffman nor Akrout teach a chip architecture having this capability or a method of making a SOC that takes advantage of this feature. As added herein, new claim 21 claims a method to manufacture a SOC that includes

> coupling a first internal bus physically located upon said single integrated circuit to said processor core and to said peripheral(s), said first internal bus has a latency tolerant signal protocol and carries signals from signal initiators to signal targets;
>
> wherein said coupling of said first internal bus further comprises adding an arbitrary number of pipeline stages between any signal initiator and any signal target when floorplanning said single integrated circuit; and
>
> wherein adding said arbitrary number of pipeline stages to said first internal bus at floorplanning does not require a subsequent design or floorplanning iteration.

Neither Hoffman, nor Akrout, nor any of the other references cited by the Examiner teach, suggest, or imply coupling an internal bus to a processor core and peripherals, where the step of coupling the bus includes adding an arbitrary number of pipeline stages in such a manner as to not require a subsequent design or floorplanning iteration. This same functional limitation on the claimed bus elements is found in all

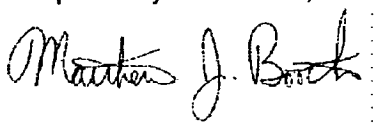
the new independent claims (claim 26, 31, and 36, claiming a method of use, an apparatus, and a system, respectively). Likewise, this same functional limitation, relating to a second internal bus element, is found in new claims 22, 27, 32, and 37, which depend from claims 21, 26, 31, and 36, respectively, and is included by dependency in new claims 23-25, 28-30, 33-35, and 38-40.

Since the new claims include elements and limitations that are not shown, taught, or implied by the prior art, Applicant therefore respectfully requests that the Examiner withdraw the claim rejections to claims 1-20 under 35 USC 103(a) as being unpatentable over Hoffman et al. (US Pat. No. 6,513,089) and Akrout et al. (US Patent Application Publication No. 2003/0115500), and further in view of Sheafor et al. (US Patent No. 6,493,407), Quereshi et al. (US Patent No. 6,173,349), Pawlowski et al. (US Patent No. 5,469,547), and Freidin et al. (US Patent No. 5,410,194).

3. Summary

In view of the above, Applicant believes that each of the presently pending claims is in immediate condition for allowance or appeal. Accordingly, Applicant respectfully requests that the Examiner withdraw the outstanding objections and rejections of the claims and issue a timely Notice of Allowance in this case.

Respectfully submitted,



Date: 9 September 2004

Matthew J. Booth
Reg. No. 35,454

Matthew J. Booth
Karen S. Wright
Booth & Wright, L.L.P.
PO Box 50010
Austin, Texas 78763-0010
Telephone: (512) 474-8488
Facsimile: (512) 474-7996
matthew.booth@boothlaw.com
karen.wright@boothlaw.com
http://www.boothlaw.com